

Overview

The circuit is an integrated low-noise-amplifier (LNA) for the 24 GHz ISM-band at 24GHz and additionally in the frequency range up to 26 GHz. It is fabricated in the IHP SiGe:C BiCMOS technology SGB25H3 by using the bipolar part only. The circuit is designed for the use in radar-systems.

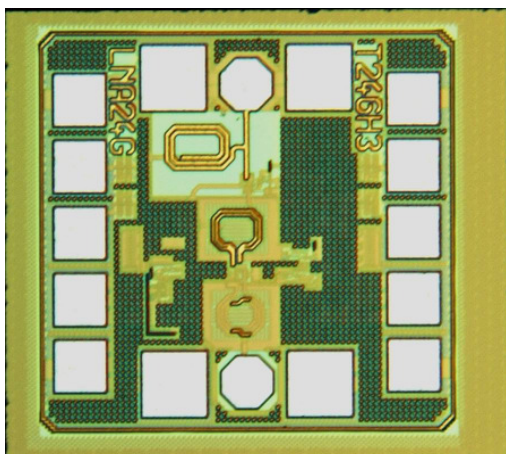
Applications

The main use of the LNA is in wireless communication systems and in radar systems for the ISM-band at 24GHz and for UWB-systems up to 26 GHz.

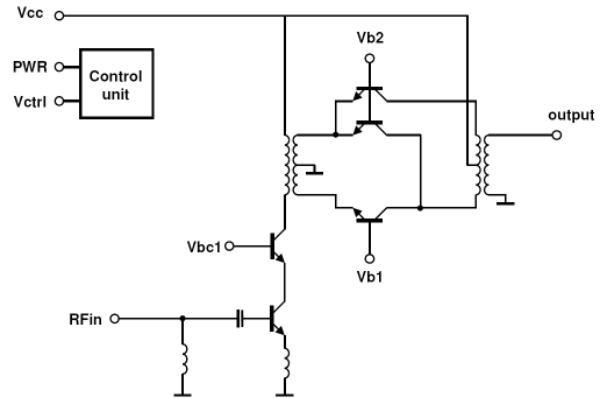
Characteristics

Parameter	24GHz LNA
Supply voltage V_{CC}	2.3 – 2.7 V
Supply current I_{CC}	4.7 mA @ 2.5V
Chip size	650x650 μm^2
Operating temp	-40°C to +95°C

Chip Photo

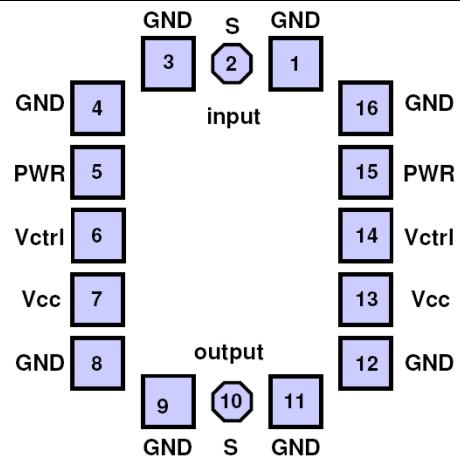


Circuit diagram



Pinout of the Chip

No.	Name	Description
1	GND	Ground, short bond to board!
2	S	RF input
3	GND	Ground, short bond to board!
4,16	GND	Ground, short bond to board!
5,15	PWR	Power down
6,14	Vctrl	switching of gain states:
7,13	V_{CC}	Supply voltage 2.5V
8,12	GND	Ground, short bond to board!
9	GND	Ground, short bond to board!
10	S	RF output
11	GND	Ground, short bond to board!



Bonding: input bond-wire $L < 0.5$ mm
 output bond-wire $L < 0.3$ mm

Description

The LNA is a two stage amplifier operating in two gain modes (HG/LG) with power down feature. The first stage employs a cascode configuration with inductive load and inductive emitter degeneration for stability reasons. The circuit diagram shown in the Figure above (for readability, the biasing and control unit are not shown). The input matching network of the LNA consist of an input pad capacitance, shunt inductor, series capacitor and a transmission line. The input shunt inductor provides also ESD protection. In order to provide compact design and galvanic isolation between amplifier stages transformers were used. The second stage is a common-base structure with fixed two gain values. This stage is also loaded with a transformer providing appropriate impedance to a loading Gilbert mixer pair. The gain mode is defined by an external digital signal Vctrl and appropriate digital circuitry (Vctrl=2.5 V – high gain, Vctrl=0 V – low gain). If high level (2.5V) is applied to PWR pin, the internal biasing circuitry is switched off and the LNA is deactivated. The simulated LNA performance is shown in the figure below.

Simulation Results

